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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/556,821	04/21/2000	Yukio Sugita	Q58959	6402
75	90 07/18/2003			
Sughrue Mion Zinn Macpeak & Seas PLLC		EXAMINER GHULAMALI, QUTBUDDIN		
2100 Pennsylvania Avenue NW Washington, DC 20037-3202				
			ART UNIT	PAPER NUMBER
			2631	5
			DATE MAILED: 07/18/2003	g

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application N	o. A	pplicant(s)
•	Office A 11 -	09/556,821		UGITA, YUKIO
	Office Action Summary	Examiner	A	rt Unit
		Qutub Ghular		631
Period fo	The MAILING DATE of this communication apor Reply	opears on the co	er sheet with the corr	respondence address
- Exte after - If the - If NO - Failu - Any	ORTENED STATUTORY PERIOD FOR REP. MAILING DATE OF THIS COMMUNICATION nsions of time may be available under the provisions of 37 CFR 1 SIX (6) MONTHS from the mailing date of this communication. Period for reply specified above is less than thirty (30) days, a report of period for reply is specified above, the maximum statutory period reply within the set or extended period for reply will, by stature to reply within the set or extended period for reply will, by stature to reply within the set or extended period for reply will, by stature the mail of patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, hi ply within the statutory of will apply and will exp	owever, may a reply be timely minimum of thirty (30) days will re SIX (6) MONTHS from the	filed I be considered timely. mailing date of this communication.
1)🖂	Responsive to communication(s) filed on 05	May 2003		
2a)□		his action is non	final	
3)	Since this application is in condition for allow			
,	closed in accordance with the practice under on of Claims	Ex parte Quay	e, 1935 C.D. 11, 453	O.G. 213.
4)🖂	Claim(s) 1-24 is/are pending in the applicatio	n.		
•	4a) Of the above claim(s) is/are withdra	wn from conside	eration.	
	Claim(s) is/are allowed.			
6)⊠	Claim(s) <u>1-24</u> is/are rejected.			
7)	Claim(s) is/are objected to			
8)[Claim(s) are subject to restriction and/o	or election requir	ement.	
	on Papers			
9)□ T	he specification is objected to by the Examine	er.		
10)∐ T	he drawing(s) filed on is/are: a)□ acce	pted or b)☐ objed	ted to by the Examine	er.
	Applicant may not request that any objection to the	e drawing(s) be he	eld in abeyance. See 3	7 CFR 1.85(a).
11) 🔲 T	he proposed drawing correction filed on	_ is: a)∏ approv	ed b) disapproved	by the Examiner.
	If approved, corrected drawings are required in re		ction.	
	he oath or declaration is objected to by the Ex	aminer.		
Priority u	nder 35 U.S.C. §§ 119 and 120			
13) 🗌 📝	Acknowledgment is made of a claim for foreigr	n priority under 3	5 U.S.C. § 119(a)-(d)	or (f).
a)[All b) Some * c) None of:			
•	 Certified copies of the priority document 	s have been rec	eived.	
2	2. Certified copies of the priority document	s have been rec	eived in Application N	lo
	B. Copies of the certified copies of the prior application from the International Buse the attached detailed Office action for a list	reau (PCT Rule	17 2(a)) [.]	this National Stage
14) 🗌 Ac	knowledgment is made of a claim for domesti	c priority under 3	5 U.S.C. § 119(e) (to	a provisional application
a)	☐ The translation of the foreign language pro cknowledgment is made of a claim for domesti	visional applicat	on has been received	d.
Notice Informa	of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) ation Disclosure Statement(s) (PTO-1449) Paper No(s)	4)	Interview Summary (PTC Notice of Informal Patent Other:	0-413) Paper No(s) Application (PTO-152)
Patent and Trad O-326 (Rev.	0.4 0.00	ion Summary	0-4-	of Paner No. 5

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DETAILED ACTION

Response to Arguments

- 1. This Office Action is responsive to the Amendment filed on 6/11/03.
- 2. Applicant's arguments with respect to claims 1-4, 6, 11-20 have been considered but are moot in view of the new ground(s) of rejection.

The rejection is as follows:

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 4. Claims 1-4, 11-14, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Mutoh (US Patent No. 5,940,101 new art);

Mutoh teaches a clock generation device for generating a first clock signal CLK, an operation device CG which operates the first clock signal and generates at least one processing clock whose phase is different than a phase of the first clock with the excitation signal PCLK of the phase θ selected by the multiplexer MP, a pulse width modulator PM for converting the image data into a pulse width signal corresponding to a density gradation, a synchronizing circuit SC for synchronizing a rising or falling edge of the output of the pulse width modulator PM with the rising or falling edge of the excitation signal PCLK from the frequency divider FD, and a

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high voltage switch (selector) for amplifying and applying the output of the synchronizing circuit SC to the control electrode 4, the delayed pulse generator DG receives the excitation signal PCLK and the reference clock signal CLK as input data and an input shift clock signal, respectively, and plurality of outputs N pulse trains, having a period of the excitation signal PCLK successively delayed by $2\pi/N$ (col. 1, lines 15-63, col. 11, lines 40-60).

5. Claims 7, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Woodworth (US Patent No. 5,991,041 new art);

Woodworth teaches the line scan camera 70, 72 used in the preferred embodiment receives a Master Clock (MCLK) signal and a Line Transfer (LT) signal, as shown in FIG. 9. The master clock is derived from a crystal oscillator, which also feeds the TCR2 input to the TPU. The line transfer signals are generated using the SPWM functions of the TPU referenced to TC2, a light source for exposure, which emits light in accordance with a pulse width of respective pulses. Woodworth therefore teaches the claim recitation. (see col. 6, lines 31-44; col. 8, lines 56-65; col. 10, lines 59-67).

Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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7. Claims 5, 6, 15, 16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mutoh (US Patent No. 5,940,101 new art) in view of Mutoh (US Patent No. 5,583,552 new art).

As applied to claims 5, 6, 15, 16, and 22 above, Mutoh teaches every feature of the claimed invention, but does not explicitly teach said operation device is an inverting device which inverts the first clock signal and generates a second clock signal. In the same field of endeavor, Mutoch (US Patent 5,583,552) teaches (fig. 3), the start position delay circuit SD is constructed, for example, from a preset decrementing counter 31, a delay type flip-flop 32, an invertor 33 and an AND gate 34. In the start position delay circuit SD, the preset decrementing counter 31 is loaded with start position delay data, which increase in proportion to a delay time, in response to a shaft encoder output (origin pulse) and is decremented in response to a registration adjusting clock signal SCLK as seen from fig. 4. When the count value of the present decrementing counter 31 is decremented finally to "ALL ZERO", a rising signal GATEPULSE is produced by the delay type flip-flop 32. Such rising signal GATEPULSE and the registration adjusting clock SCLK are ANDed by the AND gate 34 to obtain a registration adjusting clock SCLK. Referring now to fig. 5, the synchronizing circuit SC is constructed, for example, from a pair of delay type flip-flops 41 and 42. In the synchronizing circuit SC, a picture element recording clock DCLK is produced which has rising and falling edges synchronized with rising edges of a registration adjusting clock SCLK and an exciting clock PCLK, respectively, as seen from fig. 6 (col. 13, lines 40-58; col. 17, lines 10-24, lines 59-62; col. 18, lines 55-57).

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8. Similarly, claims 8-10, 18-20, 23, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woodworth (US Patent No. 5,991,041 new art) in view of Mutoh (US Patent No. 5,583,552 new art);

Woodworth teaches every feature of the claimed invention, but does not explicitly teach said operation device is an inverting device, which inverts the first clock signal and generates a second clock signal. In the same field of endeavor, Mutoch (US Patent 5,583,552) teaches (fig. 3), the start position delay circuit SD is constructed, for example, from a preset decrementing counter 31, a delay type flip-flop 32, an invertor 33 and an AND gate 34. In the start position delay circuit SD, the preset decrementing counter 31 is loaded with start position delay data, which increase in proportion to a delay time, in response to a shaft encoder output (origin pulse) and is decremented in response to a registration adjusting clock signal SCLK as seen from fig. 4. When the count value of the present decrementing counter 31 is decremented finally to "ALL ZERO", a rising signal GATEPULSE is produced by the delay type flip-flop 32. Such rising signal GATEPULSE and the registration adjusting clock SCLK are ANDed by the AND gate 34 to obtain a registration adjusting clock SCLK. Referring now to fig. 5, the synchronizing circuit SC is constructed, for example, from a pair of delay type flip-flops 41 and 42. In the synchronizing circuit SC, a picture element recording clock DCLK is produced which has rising and falling edges synchronized with rising edges of a registration adjusting clock SCLK and an exciting clock PCLK, respectively, as seen from fig. 6 (col. 13, lines 40-58; col. 17, lines 10-24, lines 59-62; col. 18, lines 55-57).

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Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (703) 305-7868. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are 703 305-3988 for regular communications and 703 305-3988 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-4750.

QG. July 14, 2003

DON N. VO PRIMARY EXAMINER